



PC-Light Control Light@Night

Data transfer via parallel port with the Interface LI-LPT

Brief description:

The **Light-Interface LI-LPT** for the parallel interface port of a computer and as a minimum one **Light-Display** or **Light-Power-Module** will be the required hardware for the **PC-Light Control Light@Night**.

Opto-couplings on the **Light-Interface LI-LPT** guaranties that there is no electrical conductive connection between PC and the light wirings at the model railway layout.

Several **Light-Display-** and **Light-Power Modules** with 40 respectively 24 light-control outputs each can be controlled by a **Light-Interface LI-LPT**.

The **Light-Display-** and **Light-Power-Module** contain shift register. Therefore is it possible to switch single outputs on or off via the **Light-Interface LI-LPT** respectively via the parallel interface port of a computer.

Appointed data lines of the parallel port:

Data bit D0: Clock
Data bit D1: Strobe
Data bit D2: Data
Data bit D7: Output Enable (+)
Select Input: Output Enable (-)

Activate or deactivate all outputs together (Output Enable):

All outputs of the **Light-Display-Module** can be switched together on or off via the parallel port lines **Data bit D7** and **Select Input**

To make sure that the connected light emitting diodes and the incandescent lamps will not be switched on or off by random without running PC-software, all outputs can be common activated during the start of the software and deactivated during ending.

Activating the outputs (program start) : Data bit D7 = high and Select Input = low.
Deactivating the outputs (program end) : Data bit D7 = low.

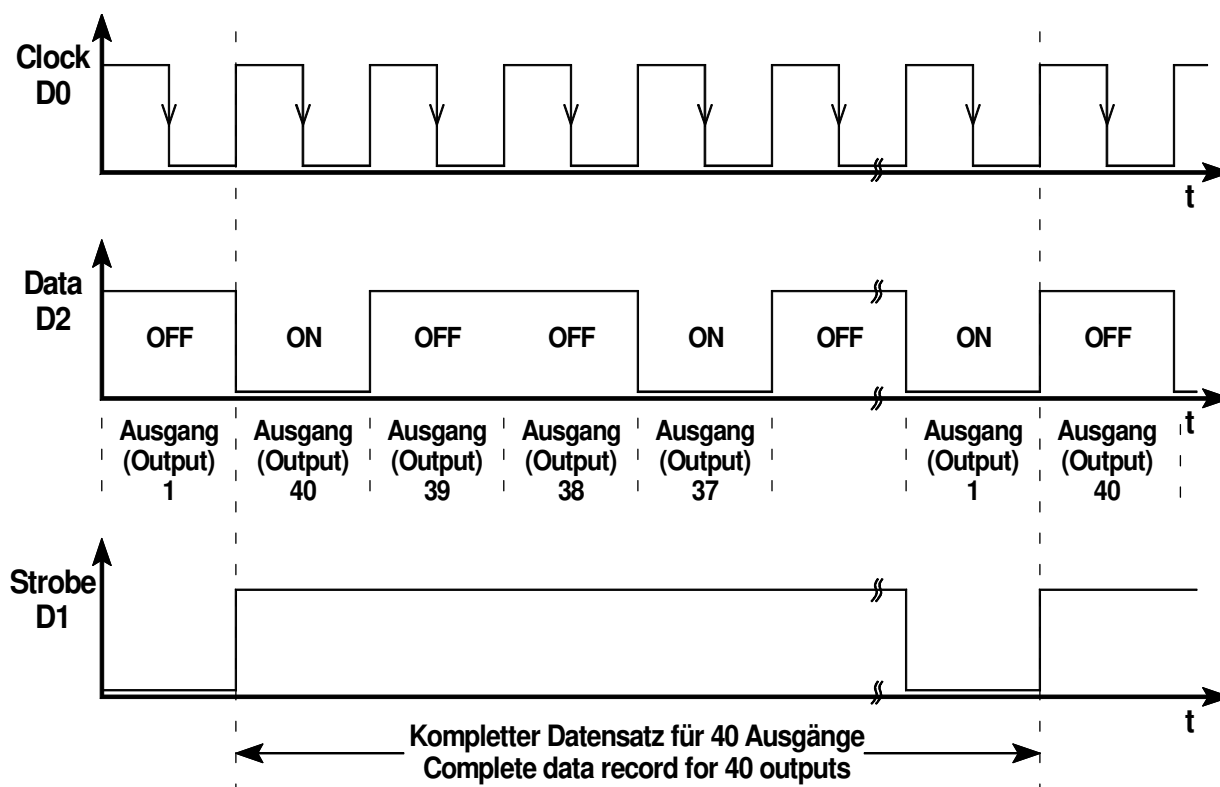
Timing Diagram:

The **quantity of clock impulses** is related to the **quantity of Light-Display- and Light-Power-Modules** which are connected to the **Light-Interface LI-LPT**. Each **Light-Display-Module** requires **40 clock impulses** and each **Light-Power-Module 24 clock impulses** to fill the shift register with data for the single outputs.

As the data will slide deeper into the shift register by any **clock-impulse** (the **active edge** is **negative** from the sight of the PC), the data transfers will always **starts with the content of the last output** and **ends with the content of the first output**.

At the end of the transfer all data will be transferred to the outputs of the shift register, **simultaneous** together with the content of the first output and therefore transferred to the outputs of the **Light-Display- respectively Light-Power-Modules** via the **strobe impulse**.

The following **Timing Diagram** shows the cohesion for the case that **one Light-Display-Module** with **40 outputs** has been connected to a **Light-Interface LI-LPT**. All logic levels are the status of the **data lines of the parallel port**.



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